WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device, the method comprising:
forming an opening in a dielectric layer;
depositing copper (Cu) or a Cu alloy to fill the opening; and
laser thermal annealing the deposited Cu or Cu alloy in ammonia (NH_3).

2. The method according to claim 1, comprising laser thermal annealing by impinging a pulsed laser light beam on the deposited Cu or Cu alloy at a radiant fluence of about 0.28 to about 0.34 joules/cm^2.

3. The method according to claim 2, comprising laser thermal annealing to heat the deposited Cu or Cu alloy to a temperature of about 983°C to about 1183°C, thereby reflowing the deposited Cu or Cu alloy.

4. The method according to claim 1, comprising laser thermal annealing employing an NH_3 flow rate of about 200 to about 2,000 sccm.

5. The method according to claim 1, comprising depositing a barrier layer lining the opening before depositing the Cu or Cu alloy.

6. The method according to claim 5, wherein the barrier layer is a composite comprising a tantalum nitride layer on the dielectric layer, a layer of alpha-tantalum (α -Ta) on the tantalum nitride layer.

7. The method according to claim 5, comprising depositing a seedlayer on the barrier layer.

8. The method according to claim 7, comprising depositing the Cu or Cu alloy by electroless plating or electroplating.

9. The method according to claim 6, comprising conducting chemical mechanical polishing (CMP) such that an upper surface of the deposited Cu or Cu alloy is substantially co-planar with an upper surface of the dielectric layer.

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10. The method according to claim 9, comprising:
treating the upper surface of the Cu or Cu alloy in a plasma containing NH_4 to remove copper oxide therefrom; and

depositing a silicon nitride capping layer on the plasma treated surface by plasma enhanced chemical vapor deposition.

11. The method according to claim 1, comprising conducting chemical mechanical polishing (CMP) such that an upper surface of the deposited Cu or Cu alloy is substantially co-planar with an upper surface of the dielectric layer.

12. The method according to claim 11, comprising:

treating the upper surface of the Cu or Cu alloy in a plasma containing NH_3 to remove copper oxide therefrom; and

depositing a silicon nitride capping layer on the plasma treated surface by plasma enhanced chemical vapor deposition.

13. The method according to claim 1, wherein the opening is a dual damascene opening containing a lower via hole section in communication with an upper trench section, the method comprising depositing the Cu or Cu alloy to fill the opening to form an upper line in communication with an underlying via.

14. The method according to claim 13, wherein the dielectric layer comprises an oxide.

15. The method according to claim 14, where the oxide is a fluorine-containing silicon oxide derived from fluorine-doped tetraethyl orthosilicate.

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